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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/636,181	08/07/2003	Andrei Mihnea	400.237US01	1762
27073	7590	06/09/2005	EXAMINER	
LEFFERT JAY & POLGLAZE, P.A. P.O. BOX 581009 MINNEAPOLIS, MN 55458-1009			PHAM, LY D	
			ART UNIT	PAPER NUMBER
			2827	
DATE MAILED: 06/09/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No. 10/636,181	Applicant(s) MIHNEA ET AL.	
	Examiner Ly D. Pham	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2005.
 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
 4a) Of the above claim(s) 8-14 is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☒ Claim(s) 1-7 is/are rejected.
 7) ☐ Claim(s) _____ is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☒ The drawing(s) filed on 28 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5-18-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1 – 7 in the reply filed on March 30, 2005 is acknowledged. The traversal is on the ground(s) that claim 1 is generic for claims 1 – 14. This is not found persuasive because claim 2, which depends on claim 1, discloses the recovery operation by ramping the gate voltage and coupling a first source/drain and a second source/drain regions to first and second constant voltages, respectively, whereas claim 8 discloses the recovery operation which floats one of the source/drain regions. Accordingly, if claim 1 is found allowable, the Election/Restriction would be withdrawn, and claims 1 – 14 allowed. Otherwise, the requirement is still deemed proper and is therefore made FINAL.

Applicants have cancelled claims 15 – 21.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohba et al. (US Pat 6,330,192 B1) in view of Chung (US Pat Pub 2004/0185619 A1).

Regarding **claim 1**, Ohba et al. disclose a method for erasing a read-only-memory (ROM) block comprising a plurality of memory cells (col. 10, lines 61 – 64) each having a gate input and two source/drain regions, the method comprising:

performing a recovery operation after erasing the memory block of the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased (col. 12, lines 22 – 29).

Although Ohba et al. did not clearly refer the ROM block as a NROM, as claimed in claim 1, however, the feature has been shown by Chung (paragraph 0010).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to utilize the NROM in corporation with the disclosure by Ohba et al. due to the advantages disclosed by Chung (paragraphs 0006 and 0009).

As per **claim 7**, Chung further disclose the NROM embedded in a CMOS device (paragraph 0009).

4. Claims 1, 2, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (US Pat 6,160,739) in view of Chung (US Pat Pub 2004/0185619 A1).

Regarding **claims 1 and 2**, Wong discloses a method for erasing a EPROM block comprising a plurality of memory cells (fig. 1) each having a gate input (fig. 1, gates connected to word lines) and two source/drain regions (fig. 1, one connected to the source line SLN and the other connected to bit line BLN), the method comprising:

erasing the memory block (col. 3, line 66 – col. 4, line 2); and

performing a recovery operation after erasing the memory block of the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased (col. 3, lines 16 – 20), the recovery operation includes biasing each of the plurality of memory cells with a ramped voltage on the gate input, a constant voltage on a first source/drain region and the remaining source/drain to a second constant voltage (col. 13, lines 23 – 25).

Although Wong did not clearly refer the EPROM block as a NROM, as claimed in claim 1, however, the feature has been shown by Chung (paragraph 0010). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to utilize the NROM in corporation with the disclosure by Wong for the advantages disclosed by Chung (paragraphs 0006 and 0009).

Regarding **claims 5 and 6**, Wong also discloses the first constant voltage in a range of 3 – 7V and the second constant voltage in a range of 0 – 3V (col. 1, lines 26 – 39).

As per **claim 7**, Chung further disclose the NROM embedded in a CMOS device (paragraph 0009).

5. Claims 1 – 4, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haddad et al. (US Pat 6,172,909 B1) in view of Chung (US Pat Pub 2004/0185619 A1).

Regarding **claims 1 and 2**, Haddad et al. disclose a method for erasing a EEPROM block comprising a plurality of memory cells (fig. 1A) each having a gate input

(fig. 1, gates connected to word lines) and two source/drain regions (fig. 1, one connected to the source line to the power source 106, and the other connected to bit line to bit line driver 102), the method comprising:

erasing the memory block (col. 3, lines 7 – 19); and

performing a recovery operation after erasing the memory block of the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased (abstract: soft programming for over-erased cells..., and col. 5, lines 25 – 40), the recovery operation includes biasing each of the plurality of memory cells with a ramped voltage on the gate input (col. 5, lines 41 – 45), a constant voltage on a first source/drain region and the remaining source/drain to a second constant voltage (abstract).

Although Haddad et al. did not clearly refer the EEPROM block as a NROM, as claimed in claim 1, however, the feature has been shown by Chung (paragraph 0010). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to utilize the NROM in corporation with the disclosure by Haddad et al. for the advantages disclosed by Chung (paragraphs 0006 and 0009).

Regarding **claim 3**, Haddad et al. also disclose the method of claim 1, wherein the ramped voltage applies to the gate Is in a range of 0V to 3V (abstract: $V_{gs} < 3V$).

Regarding **claim 4**, Haddad et al. also disclose the method of claim 1, wherein the ramp voltage has a time period in a range of 10us to 1sec from start to end (col. 10, lines 44 – 47, ‘... <200msec in addition to the typical 0.5 to 1.0 second erase time per sector’).

As per **claim 7**, Chung further disclose the NROM embedded in a CMOS device (paragraph 0009).

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohba et al. and Chung, and further in view of Mehrad (US Pat 5,576,992).

Regarding **claim 2**, Ohba et al. and Chung disclose a method for erasing a NROM block except wherein the recovery operation includes coupling the gate input to a ramped voltage, a first source/drain region to a first constant voltage, and the remaining source/drain to a second constant voltage. However, this feature has been shown by Mehrad (col. 2, lines 7 – 9, col. 6, lines 12 – 25, and table 1, where selected word line voltage is ramped).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature shown by Mehrad to the disclosure by Ohba et al., so that programming operations for recovering the over-erased cells does not damage the oxide gate insulators of the cells (Mehrad col. 2, lines 58 – 67).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
June 6, 2005



**TAN T. NGUYEN
PRIMARY EXAMINER
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